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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,796	12/09/2003	Michael Kilian	E0295.70196US00	4319

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,796	KILIAN ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Figures 1-7 are hand-written. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-24 are rejected under U.S.C. 102(e) as being anticipated by Pandya (US PGPub 2004/0030806).

Claim 1. A method of processing data in a computer system comprising at least one host and at least one content addressable storage system which stores data for the at least one host, *(Section 0163, lines 1-2 – State that the host transfers data to the system buffer memory. Section 0118, line 10 – Denotes a content addressable memory)*

- wherein the at least one host accesses data units stored on the at least one storage system using content addresses generated based on the content of the data units, the method comprising: *(Section 0121, lines 76-100 – Describe how the one host accesses data units stored on the at least one storage system using content addresses generated based on the content of the data units. Section 0121, lines 27-29 – State that the engines receive the write data from the host)*
- (a) maintaining at least one index that maps a content address of at least one data unit to a storage location within the at least one storage system at which the data unit is stored; and *(Section 0128, lines 11-14 - If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)*
- (b) maintaining a cache of the location index. *(Section 0128, lines 7-11 – State the following: "The session cache look-up engine, block 2904, provides the functionality to look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry.")*

Claim 2. The method of claim 1, wherein the act (a) comprises an act of maintaining the location index on at least one magnetic disk, and *(Section 0092, lines 6-7 – State that there is a disk array.)*

- the act (b) comprises an act of maintaining the cache in a random access memory. *(Section 0106, lines 14-22 – State the following: "The disclosed processor includes a memory subsystem, including a*

memory controller interface, which manages the on chip session cache/memory, and a memory controller, block 1602, which manages accesses to the off chip memory which may be SRAM, DRAM, FLASH, ROM, EEPROM, DDR SDRAM, RDRAM, FCRAM, QDR SRAM, or other derivatives of static or dynamic random access memory or a combination thereof.")

Claim 3. The method of claim 1, wherein the at least one storage system includes at least one storage node *(Section 0124, lines 84-86 – Denote storage nodes)*

- having at least one storage device and at least one access node that processes access requests from the at least one host, *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes)*
- and wherein the act (b) further comprises an act of maintaining the cache on the at least one storage node. *(Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

Claim 4. The method of claim 1, wherein the at least one storage system includes at least one storage node having at least one storage device and at least one access node that processes access requests from the at least one host, and *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes. Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

- wherein the act (b) further comprises an act of maintaining the cache on the at least one access node. *(Section 0124, lines 18-100 – Show how a cache is maintained on at least one access node)*

Claim 5. The method of claim 1, wherein the at least one storage system comprises a plurality of storage nodes for storing data received from the at least one host, *(Section 0163, lines 1-2 – State that the host transfers data to the system buffer memory. Section 1024, lines 7-100 – State the following: "Then the data transfer between the two nodes can continue without host*

processor intervention, as long as the available buffer space and buffer transfer credits are maintained by the two end nodes.)

- and wherein the at least one index is stored, at least in part, on at least two of the plurality of storage nodes. *(Section 0124, lines 18-100 – Show how at least one index is stored on 2 storage nodes)*

Claim 6. The method of claim 5, wherein a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored. *(Section 0124, lines 18-100 – Show how a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored)*

Claim 7. The method of claim 6, wherein the cache of the location index is stored on a single one of the plurality of storage nodes. *(Section 0128, lines 26-30 – State the following: "The session memory may be single way or multi-way cache or a hash indexed memory or a combination thereof, depending on the silicon real estate available in a given process technology.")*

Claim 8. The method of claim 5, wherein the storage system comprises a plurality of access nodes and the cache of the location index is stored on at least one of the plurality of access nodes. *(Section 0124, lines 18-100 – Show how a cache of the location index is stored on at least one access node. Section 0128, lines 7-14 - The session cache look-up engine, block 2904, provides the functionality to look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry. If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)*

Claim 9. At least one computer readable medium encoded with instructions that, when executed on a computer system, perform a method of processing data, *(Section 0119 – Denotes a processor that is encoded with data processing instructions)*

- wherein the computer system comprises at least one host and at least one content addressable storage system which stores data for the at least one host, and wherein the at least one host accesses data units stored on the at least one storage system using content addresses generated based on the content of the data units, the method comprising: *(Section 0121, lines 76-100 – Describe how the one host accesses data units stored on the at least one storage system using content addresses generated based on the content of the data units. Section 0121, lines 27-29 – State that the engines receive the write data from the host)*
- (a) maintaining at least one index that maps a content address of at least one data unit to a storage location within the at least one storage system at which the data unit is stored; and *(Section 0128, lines 11-14 - If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)*
- (b) maintaining a cache of the location index. *(Section 0128, lines 7-11 - The session cache look-up engine, block 2904, provides the functionality to look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry.)*

Claim 10. The at least one computer readable medium of claim 9, wherein the act (a) comprises an act of maintaining the location index on at least one magnetic disk, *(Section 0092, lines 6-7 – State that there is a disk array.)*

- the act (b) comprises an act of maintaining the cache in a random access memory. *(Section 0106, lines 14-22 – State the following: "The disclosed processor includes a memory subsystem, including a memory controller interface, which manages the on chip session cache/memory, and a memory controller, block 1602, which manages accesses to the off chip memory which may be SRAM, DRAM, FLASH, ROM, EEPROM, DDR SDRAM, RDRAM, FCRAM, QDR SRAM, or other derivatives of static or dynamic random access memory or a combination thereof.")*

Claim 11. The at least one computer readable medium of claim 9, wherein the at least one storage system includes at least one storage node *(Section 0124, lines 84-86 – Denote storage nodes)*

- having at least one storage device and at least one access node that processes access requests from the at least one host, *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes)*
- and wherein the act (b) further comprises an act of maintaining the cache on the at least one storage node. *(Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

Claim 12. The at least one computer readable medium of claim 9, wherein the at least one storage system includes at least one storage node having at least one storage device and at least one access node that processes access requests from the at least one host, and *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes. Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

- wherein the act (b) further comprises an act of maintaining the cache on the at least one access node. *(Section 0124, lines 18-100 – Show how a cache is maintained on at least one access node)*

Claim 13. The at least one computer readable medium of claim 9, wherein the at least one storage system comprises a plurality of storage nodes for storing data received from the at least one host, *(Section 0163, lines 1-2 – State that the host transfers data to the system buffer memory. Section 1024, lines 7-100 – State the following: "Then the data transfer between the two nodes can continue without host processor intervention, as long as the available buffer space and buffer transfer credits are maintained by the two end nodes.)*

- and wherein the at least one index is stored, at least in part, on at least two of the plurality of storage nodes. *(Section 0124, lines 18-100 – Show how at least one index is stored on 2 storage nodes)*

Claim 14. The at least one computer readable medium of claim 13, wherein a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored. *(Section 0124, lines 18-100 – Show how a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored)*

Claim 15. The at least one computer readable medium of claim 14, wherein the cache of the location index is stored on a single one of the plurality of storage nodes. *(Section 0128, lines 26-30 – State the following: "The session memory may be single way or multi-way cache or a hash indexed memory or a combination thereof, depending on the silicon real estate available in a given process technology.")*

Claim 16. The at least one computer readable medium of claim 13, wherein, the storage system comprises a plurality of access nodes and the cache of the location index is stored on at least one of the plurality of access nodes. *(Section 0124, lines 18-100 – Show how a cache of the location index is stored on at least one access node. Section 0128, lines 7-14 - The session*

cache look-up engine, block 2904, provides the functionality to look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry. If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)

Claim 17. A content addressable storage system for use in a computer system, that includes the content addressable storage system and at least one host, *(Section 0163, lines 1-2 – State that the host transfers data to the system buffer memory. Section 0118, line 10 – Denotes a content addressable memory)*

- wherein the at least one host accesses data units stored on the content addressable storage system using content addresses generated based on the content of the data units, the content addressable storage system comprising: *(Section 0121, lines 76-100 – Describe how the one host accesses data units stored on the at least one storage system using content addresses generated based on the content of the data units. Section 0121, lines 27-29 – State that the engines receive the write data from the host)*
- at least one storage device to store data received from the at least one host; and at least one controller that: maintains at least one index that maps a content address of at least one data unit to a storage location within the content addressable storage system at which the data unit is stored; and *(Section 0128, lines 11-14 - If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)*
- maintains a cache of the location index. *(Section 0128, lines 7-11 - The session cache look-up engine, block 2904, provides the functionality to*

look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry.)

Claim 18. The content addressable storage system of claim 17, wherein the at least one controller maintains the location index on at least one magnetic disk *(Section 0092, lines 6-7 – State that there is a disk array.)*

- and maintains the cache in at least one random access memory. *(Section 0106, lines 14-22 – State the following: "The disclosed processor includes a memory subsystem, including a memory controller interface, which manages the on chip session cache/memory, and a memory controller, block 1602, which manages accesses to the off chip memory which may be SRAM, DRAM, FLASH, ROM, EEPROM, DDR SDRAM, RDRAM, FCRAM, QDR SRAM, or other derivatives of static or dynamic random access memory or a combination thereof.")*

Claim 19. The content addressable storage system of claim 17, further comprising at least one storage node *(Section 0124, lines 84-86 – Denote storage nodes)*

- having at least one storage device and at least one access node that processes access requests from the at least one host, *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes)*
- and wherein the act (b) further comprises an act of maintaining the cache on the at least one storage node. *(Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

Claim 20. The content addressable storage system of claim 17, further comprising at least one storage node having the at least one storage device and at least one access node that processes access requests from the at least one host, *(Section 0124, lines 93-100 – State that the host requests access, which gets processed by access nodes. Section 0128, lines 30-45 – Claim that there is a cache on at least one storage node)*

- wherein the at least one controller maintains the cache on the at least one access node. *(Section 0124, lines 18-100 – Show how a cache is maintained on at least one access node)*

Claim 21. The content addressable storage system of claim 17, further comprising a plurality of storage nodes for storing data received from the at least one host, *(Section 0163, lines 1-2 – State that the host transfers data to the system buffer memory. Section 1024, lines 7-100 – State the following: "Then the data transfer between the two nodes can continue without host processor intervention, as long as the available buffer space and buffer transfer credits are maintained by the two end nodes.)*

- and wherein the at least one index is stored, at least in part, on at least two of the plurality of storage nodes. *(Section 0124, lines 18-100 – Show how at least one index is stored on 2 storage nodes)*

Claim 22. The content addressable storage system of claim 21, wherein a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored. *(Section 0124, lines 18-100 – Show how a number of the plurality of storage nodes on which the cache of the location index is stored is less than a number of the plurality of storage nodes on which the at least one location index is stored)*

Claim 23. The content addressable storage system of claim 22, wherein the cache of the location index is stored on a single one of the plurality of storage nodes. *(Section 0128, lines 26-30 – State the following: "The session memory may be single way or multi-way cache or a hash indexed memory or a combination thereof, depending on the silicon real estate available in a given process technology.")*

Claim 24. The content addressable storage system of claim 21, wherein the storage system comprises a plurality of access nodes and the cache of the location index is stored on at least one of the plurality of access nodes. *(Section 0124, lines 18-100 – Show how a cache of the location index is stored on*

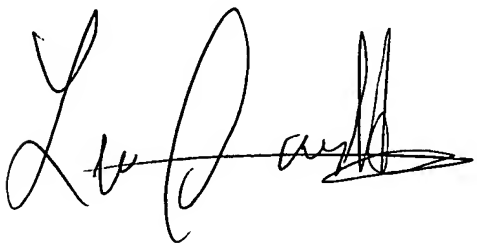
at least one access node. Section 0128, lines 7-14 - The session cache look-up engine, block 2904, provides the functionality to look-up a specific session cache entry. This look-up block creates a hash index out of the fields provided or is able to accept a hash key and looks-up the session cache entry. If there is no tag match in the cache array with the hash index, the look-up block uses this key to find the session entry from the external memory and replaces the current session cache entry with that session entry.)

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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